Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Previously presented) An instruction controlled data processing device comprising:

an instruction issue unitthat is configure(Previously presented) d to issue respective ones of instructions of program code in successive instruction cycles, the instructions including at least a first type of instruction and a second type of instruction;

a clocking circuit that is configured to clock the instruction cycles;

a register file with a read port and a write port;

a plurality of functional units, each functional unit having a control input coupled to the issue unit, an operand input coupled to the read port and a result output coupled to the write port; and

a control unit coupled to the issue unit, that is configured to route the result output of a first functional unit to the write port of the register file in response to instructions of the first type, and to the operand input of a second functional unit during an instruction cycle in response to instructions of the second type;

wherein the clock circuit is configured to vary a rate of clocking the instruction cycles in dependence upon whether a current segment of the program code includes one or more instructions of the second type.

2. (Previously presented) The processing device of claim 1, organized as a VLIW processor, wherein the issue unit includes a plurality of issue slots for issuing a VLIW instruction word, the register file having a plurality of sets of read and write ports, the functional units or groups of functional units each coupled to a respective one of the issue slots and the sets of read and write ports.

3. (Canceled)

4. (Previously presented) The processing device of claim 1, wherein the clock circuit includes a plurality of selectable clock rates, including a first clock rate that is sufficiently slow to accommodate a latency of instructions of the second type involved in producing a result from the second functional unitduring execution of the instruction of the second type within the instruction cycle, and a second clock rate that is too fast to accommodate the latency of instructions of the second type in the instruction cycle, but accommodates latency of instructions of the first type.

5. (Previously presented) The processing device of claim 1, wherein the control unit is configured to selectively route the result output of a third functional unit to a further operand input of the second functional unit under control of the instruction of the second type.

6. (Previously presented) The processing device of claim 5, wherein the program code includes a VLIW instruction that contains a command for the third functional unit and the instruction of the second type for issue in a same instruction cycle.

7. (Previously presented) The processing device of claim 1, wherein the control unit is arranged to make the second functional unit respond to the instruction of the second type in an instruction execution cycle following an instruction execution cycle in which the first functional unit responds to the instruction of the second type.

8. (Previously presented) The processing device of claim 7, wherein the result of the first functional unit is routed without intermediate latching from the first functional unit to the operand input of the second functional unit.

9. (Canceled)

10. (Previously presented) A method of executing a processing task, comprising:

providing a plurality of functional units,

issuing successive instructions at an instruction cycle rate;

executing those of the instructions that are of a first type each with an individual one of the functional units during one instruction cycle,

executing an instruction that is of a second type with a first and a second one of the functional units in series during one instruction cycle;

routing a result of the first one of the functional units to an operand of the second one of the functional units in response to the instruction of the second type; and

selecting the instruction cycle rate from at least a first and second rate, based on the type of instruction, the first rate being so slow that execution of instructions of the second type by a cascade of at least two of the functional units fits within an instruction cycle at the first rate, the second rate being so fast that only execution of instructions of the first type fits within the instruction cycle at the second rate, execution of instructions of the second type not fitting within one instruction cycle at the second rate.

11. (Previously presented) The method of claim 10, including

issuing the successive instructions each as part of a VLIW instruction word that contains a plurality of instructions for respective further functional units;

including in the instruction word that contains the instruction of the second type a further instruction for a particular one of the further functional units; and

routing a further result of the further instruction from the particular one of the further functional units to a further operand input of the second one of the functional units in response to the instruction of the second type.

12. (Currently amended) The method of claim 10, including adapting the instructions used to execute the processing task to the selected instruction cycle rate, so that the instructions of the second type are used when the task is executed at the first rate and the instructions of the second type are replaced by instructions of the first type with corresponding effect when the task is executed at the second rate.